Redesign a 4-bit ALU circuit for glitch reduction and examine its power saving

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***Abstract*—This work aims at studying the power reduction of a 4-bit ALU by reducing the power consumed by the glitches in its operation. We propose The redesigned circuit can be used instead of the original one without any loss in operation of the device. A power saving of around 16 percent was achieved using the design without any change in the critical path delay. With a modest increase in the critical path delay more power saving of around 30 percent is also achieved. The redesigned circuits works without any errors but there will be a slight overhead in the circuit due to the addition of more delay elements.**

***Index Terms*— CMOS delay devices, CMOS logic gate design, digital integrated circuits, dynamic power, linear programming, low power design.**

I. INTRODUCTION

In the recent decade there is a big surge in the use of mobile devices. Low power has become one of the major design issues due to the increased demand in personal computing devices and wireless communication systems. These devices are getting smaller and smaller every day and can be found everywhere. The integrated circuits are going into something small like watches and fitness trackers to relatively larger devices like laptops, personal computers. No one wants to have a device which cannot run long enough to sustain days' worth of usage however good the functions of the device are. Since we are not making any significant progress in replacing lithium ion batteries we are looking into various methods to efficiently run the circuit and not make the device bigger than it already is. The consumption of power by CMOS digital circuits composes mainly of two types they are, dynamic power caused by signal transition and the power due to short-circuit current and leakage current. Among these two, dynamic power dissipation plays a major role in the dissipation of power. A glitch is caused by the spurious change in the signal state which doesn't contribute to the functioning of the circuit. Glitches contribute a vast percentage in the power wastage, eliminating them would theoretically save a lot of power.

There are many ways to perform the logic functions by combing various basic gates like NOT, AND, OR, etcetera. CMOS style is the most prominent style used in current technologies. The root problem is MOSFETs is that it is not an ideal switch. When a MOSFET is open it provides us with a large but not infinite resistance as we predict in an ideal and theoretical environment. When it is closed it doesn't provide a small current due to which a small amount of current leaks and causes power dissipation. Gate delay can be defined as the time taken for a gate to reach 50 percent of VDD after the signal at the input reaches 50 percent of VDD.

Gate sizing is a method that scales the size of the gates to change their timing behavior. Gate sizing is an effective method to achieving delay optimization and the solutions for this include using iterative solutions, algorithms, linear programming etcetera. The down scaling of a transistor makes it smaller and in turn reduces its power consumption. This is caused due to the reduction of capacitances. But scaling changes many of the transistor properties like transition delays density at the output of the gate. This decreases the load on the predecessor gates and thereby an increase in the delay of the signal propagation. The transition activity is affected by the scaling of transistors and should be considered in the optimization. Using all these methods we are trying to balance the delays of all the paths other than the critical path. The delay shouldn't increase as we don't want to compromise on the performance of the device.

We will first look at the sources of CMOS power dissipation. CMOS power dissipation will occur mostly during the change in logic states. CMOS gates can have a filtering effect under certain conditions. We used various softwares to achieve the results we want, ModelSim for writing the VHDL code for the 4-bit ALU Leonardo Spectrum for area and gate delays, Design Architect for getting the netlist of the circuit and HSPICE for getting

the power and current parameters involved in the circuit.

II. CMOS POWER DISSIPATION.

There are three sources of power dissipation in any CMOS gate.

- Dynamic power Dissipation
- Short-circuit power dissipation
- dissipation due to the leakage current.

Both Dynamic and Short-circuit power dissipation occur during state transitions and compared to the above two, the dissipation due to leakage current is much lower in the order of a thousand. The supply voltage is considered to be constant and ideal.

A. Dynamic Power Dissipation:

The dynamic power dissipation occurs due to the loading and unloading of the energy stored in the gate. The capacitance includes various sources and it is the sum of all these sources. The sources are capacitances in the gate oxides of the transistors of the gates in the fanout, wire capacitances driving the gate, capacitances driven by the gate.

The dynamic power dissipation can be calculated by the formula.

Pdynamic =1/2.(Capacitance of load).((VDD)^ 2).f.D

where

- *Pdynamic is the dynamic power dissipation*
- *f is the clock frequency*
- *Vdd is the supply voltage*
- *D is the transition density of the output of the gate*

Transition density can be defined as the number of transitions during a clock cycle.

B. Short Circuit Power Dissipation

When a gate switches from high to low or vice versa it causes a power dissipation which can be classified as short circuit power dissipation. When a transition is occurring there will arise a situation when both the pull up network and pull down are conducting, the window in which both conduct is pretty low but it is present. This momentarily causes a short circuit and energy is dissipated. The amount of energy dissipated in this window depends how fast the transistor is switching. The formula for short circuit power dissipation can be summarized as following

Pshort = ((B/12). (VDD – 2(VT)^3). t)/T

where

- Pshort is the power dissipated due to short circuit
- VDD is the supply voltage.
- VT is the threshold voltage.
- t is the time taken to for the signal to fall or rise.
- T is the period of the signal.

2.2 Glitch Model:

As we discussed above the major loss of power occurs due to the state transitions in a CMOS transistor. A glitch can be seen in the diagram below for a better understanding

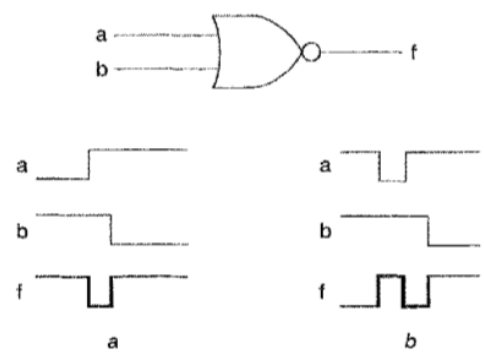

Fig.1 the two types of glitches shown above

a. Static Glitch

b. Dynamic Glitch

A glitch once created in the fan in of a circuit propagates in the circuit till the output and creates lot more glitches in the propagation. Glitch transition consumes as much power as a normal transition. Glitches are usually created when a non glitch or glitch signals arrive at different times at the input of a gate. The width of a glitch is a factor in whether the glitch is propagated or suppressed.

A glitch makes an even number of transitions on a node. If the number of signal transitions at a node for agiven input vector obtained by simulation is N, then number of transitions by glitches can be represented by

$$N_{glitch_tran} = \left\lfloor \frac{N_{tran}}{2} \right\rfloor \times 2$$

III. IMPLEMENTATION OF THE PROJECT

Initially a standard circuit 74181 made by Signetics was considered for the project. 74181 consisted of 63 gates and can do a total of 16 different functions. But due to the complexity of the circuit which consists of 30 nodes and 43 paths, the optimization was quite difficult. So we designed our own 4-bit ALU which can do only 4 functions which are Add, Subtract, Increase by 1, Decrease by 1. This makes the project to implement a little easier. Our new design has a total of 43 gates and 10 different paths.

The functions of the 4 bit ALU are shown below in the figure 2.

Select line 0	Select line 1	Function
0	0	Addition
0	1	Subtract
1	0	Increase by 1
1	1	Decrease by 1

Fig 2. Functions of the 4-bit ALU

The diagram below shows all the steps to be followed to get the result. Four different softwares namely ModelSim, Leonardo Spectrum, Design Architect, HSPICE were used.

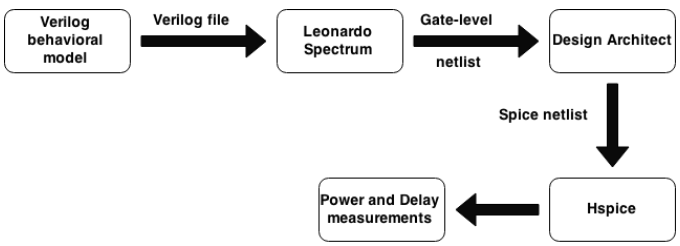

Fig 3. Flowchart of all the process involved

Step 1: The first step of the project is to write a design a 4 bit ALU which is written in VHDL and converted to Verilog.

Step 2: In this step we use the verilog code and process in Leonardo Spectrum to get the circuit area and the delays at each and every gate. The process we used is TSMC 350uM technology. This is converted to 45nm in the later stages of the project.

Step 3: In this step we use the gate level netlist generated by Leonardo Spectrum and process it in Design architect software to get a spice netlist. We also get a gate level schematic from Design architect and can verify the logic programmed in the first step. Any corrections needed are made and the above steps are repeated until we get the right logic implementation.

The below diagram shows the schematic of our 4-bit ALU designed in VHDL environment.

It contains

- 45 gates
- 10 paths to the output

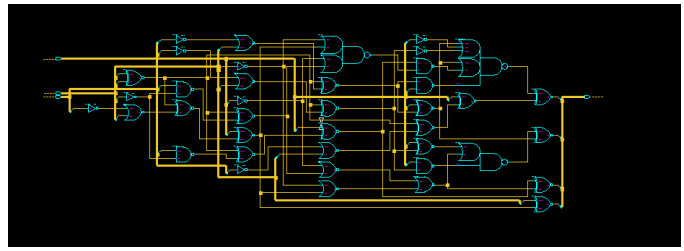

Fig 4. Schematic of the design

The above schematic shown above has a critical path delay of 1.61ns.

Step4: In this step we use the spice level netlist from the previous step and process it in HPSICE. HSPICE is used to get all the current, voltage, capacitance values involved in our circuit. The important outputs we are interested in are the power consumed by the circuit. This can show us how much power we are saving by various glitch power reduction techniques.

IV. Experimental Results

1. Original circuit results
   - Path delay: 1.61ns
   - Power consumed: 0.31577 W

2. Redesigned circuit results
   - with increase in delay
   - Path Delay: 1.76ns
   - Power consumed: 0.21627 W

We can see that there is a reduction of 28 percentage in the glitch power with an increase in critical path delay.

V. Conclusions

In this project we achieved the above results by introducing only delay buffers and not transistor scaling. By using only delay buffers and not increasing the critical path delay we gained only a modest reduction of 10 percent in the energy consumption. This is very low compared to the overhead added to the circuit by introducing delay buffers. So when the critical path delay was allowed to increase from 1.61ns we achieved a power reduction of nearly 28 percent which is satisfactory.

VI. Future Work

Even though there was a power saving of 28 percent it can be increased more and others were able to get more than 50 percent power reduction. Since only delay buffers were used and no transistors were scaled the optimization is not complete. This can be further explored and by using

Linear Programming to find the optimum solution for both delay buffers and transistor scaling we can achieve maximum power reduction possible in the circuit.

VII. Acknowledgment

I thank Dr. Agrawal for assigning me this project. It is a great way to learn the subject and verify the theoretical concepts taught in class through experiments and learn the various simulation tools available. I thank my friends for sharing their experiences with the Mentor-graphics tools to help me solve the problems I faced with those tools.

VIII. References

1. S.Kim, J.Kim and S.-Y.Hwang, " *New path balancing algorithm for glitch power reduction* "- IEE Pruc.-Circvit.s Device5 Syst., Vol. 148, No 3, June 2001

2. L. Wang, M. Olbrich, E. Barke, "A Gate Sizing Method for Glitch Power Reduction"

3. Tezaswi Raja, Member, IEEE, Vishwani D. Agrawal, Fellow, IEEE, and Michael L. Bushnell, Fellow, IEEE, "*Variable Input Delay CMOS Logic for Low Power Design*"- IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 17, NO. 10, OCTOBER 2009

4. Etienne Jacobs, "*Using Gate Sizing to Reduce Glitch Power*"

5. Masanori Hashimoto, Hidetoshi Onodera and Keikichi Tamaru , "*A Power Optimization Method Considering Glitch Reduction by Gate Sizing* "

6. E-Seok Chung ,Taewhan ,Kim C. L. Liu, "*A Non-Zero Delay Model for Glitch Analysis in Logic Circuits* " - Roc. 43rd IEEE Midwest Symp. on Circuits and Systems, Lansing MI, Aug 8- 11,2oOO

7. http://www.datasheetcatalog.com/datasheets_pdf/7/4/1/8/74181.shtml